REMARKS

Claims 30-57 and 63-70 are pending in the present application. In the Office Action, claim 43 was objected to because of an informality. Claim 43 has been amended. Applicants request that the Examiner's objection to claim 43 be withdrawn.

In the Office Action, claims 30, 45, 50, and 63 were rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi, et al (U.S. Patent No. 5,615,263). The Examiner's rejections are respectfully traversed.

Takahashi describes a dual-mode processor 12 that may be used in a secure mode or a normal mode. The dual-mode processor 12 communicates with a control channel processor 11 and a demultiplexer 13, which receives an encrypted data stream 14 and produces a demultiplexed decrypted data stream 15. See Takahashi, col. 2, ll. 28-61 and Figure 1. Upon entry to the secure mode, a hardware control circuit 26 disables input/output to the dual-mode processor 12. Upon exiting the secure mode, the hardware control circuit 26 enables input/output to the dual-mode processor 12. See Takahashi, col. 3, ll. 48-51. However, Takahashi does not describe or suggest security hardware that includes a lock override register configured to deny access to one or more secure assets when a lock override it is set, as set forth in independent claim 30 and claims depending therefrom, such as claim 45.

In response to this argument, the Examiner alleges that ROM 24 corresponds to a lock override register. Applicants respectfully disagree for the following reasons. The secure mode entry routine 51 in the ROM 24 is a software routine that may be executed when the secure mode is entered or when dual-mode processor 12 is reset. See Takahashi, col. 4, ll. 46-50 and Figure 5. Accordingly, Applicants respectfully submit that neither ROM 24 nor the secure mode entry

routine 51 are registers of any sort, much less lock override registers, as set forth in independent claim 30.

Applicants also submit that Takahashi also fails to teach or suggest receiving access to the security assets while in the first operating mode that is different from a secure mode and permitting access to the security assets in response to receiving access to the secured assets while in the first operating mode, as set forth in independent claims 50 and 63. To the contrary, the system described in Takahashi *never* grants access to ROM 24 when operating in any mode except for the secure mode.

For at least these reasons, Applicants respectfully submit that the present invention is not anticipated by Takahashi and request that the Examiner's rejections of claims 30, 45, 50, and 63 under 35 U.S.C. 102(b) be withdrawn.

In the Office Action, claims 30, 32-38, 48, 50, and 63 were rejected under 35 U.S.C. 102(e) as being anticipated by Angelo, et al (U.S. Patent No. 6,581,162), which will be referred to hereinafter as Angelo '162. The Examiner's rejections are respectfully traversed.

Angelo '162 describes a computer system that may be operated in a normal mode and a System Management Mode (SMM). While the system is in the System Management Mode, an encryption algorithm may be stored in a secure memory space that is not accessible to normal software processes that operate in the normal mode. However, Angelo '162 does not describe or suggest security hardware that includes a lock override register configured to deny access to one or more secure assets when a lock override bit is set, as set forth in independent claim 30 and claims depending therefrom, such as claims 32-38 and 48.

Angelo '162 also fails to teach or suggest receiving access to the security assets while in a first operating mode that is different from a secure operating mode and permitting access to the

security assets in response to receiving access to the secured assets while in the first operating mode, as set forth in independent claims 50 and 63. To the contrary, Angelo teaches that access to the secure memory space is granted only when the system is operating in the SMM mode and is not granted when the system is operating in any other mode.

For at least these reasons, Applicants respectfully submit that the present invention is not anticipated by Angelo '162 and request that the Examiner's rejections of claims 30, 32-38, 48, 50, and 63 under 35 U.S.C. 102(e) be withdrawn.

In the Office Action, the Examiner objected to claims 40-43, 54, 56, 67, and 69 as being dependent upon a rejected base claim, but indicated that these claims contain allowable subject matter. Pursuant to the above arguments, Applicants respectfully submit that claims 40-43, 54, 56, 67, and 69 are in condition for allowance.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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